PENDING CLAIMS AND STATUS THEREOF

Claim 1 (canceled)

2. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1010 kkkk kkkk, wherein upon invocation of the instruction, an 8 bit literal is copied to the location pointed to by a file select register, and the file select register is then decremented, the literal 'k' is designated in the kkkk kkkk portion of the instruction.

3. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1001 ffkk kkkk, wherein upon invocation of the instruction, a 6 bit unsigned literal is subtracted from a file select register to form a result, the result being stored into the file select register, the literal being designated in the kk kkkk portion of the instruction, the file select register begin designated in the ff portion of the instruction.

4. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1001 11kk kkkk, wherein upon invocation of the instruction, an unsigned 6 **[[big]]** **bit** literal is subtracted from a file select register to form a result, the result being stored back into the file select register and returned, the literal being designated in the kk kkkk portion of the instruction.

5. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1000 ffkk kkkk, wherein upon invocation of the instruction, an unsigned 6 bit literal is added to a file select register, the result being stored into the file select register, the literal being designated in the kk kkkk portion of the instruction, the file select register being designated in the ff portion of the instruction.

6. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1000 11kk kkkk, wherein upon invocation of the instruction, a 6 bit literal designated by the kk kkkk portion of the instruction is added to a file select register and the result is stored back into the file select register.

7. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1011 0sss ssss 1111 dddd dddd dddd, wherein upon invocation of the instruction, an 8 bit value is copied to a destination designated by the 12 bit value dddd dddd dddd, the location of the 8 bit value that is copied to the destination is designated by adding the 7 bit literal value sss ssss to the value in a file select register.

8. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 1110 1011 1sss ssss 1111 xxxx xddd dddd, wherein upon invocation of the instruction, an 8 bit value is copied to a location designated by ddd dddd portion of the instruction, the location of the 8 bit value is determined by adding the 7 bit literal value sss ssss to the value in a file select register.

9. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 0000 0000 0001 0100, wherein upon invocation of the instruction, an address of a next instruction is pushed onto a hardware stack.

10. **(currently amended):** A microcontroller ~~**as in claim 1**~~ **comprising:**

a central processing unit;

a data memory having a linearized address space coupled with the central processing unit being divided into *n* banks;

the central processing unit comprising:

a bank select unit which either accesses one of the banks or accesses a virtual bank, whereby the virtual bank combines partial memory space of

two banks of the data memory and wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file;

a plurality of special function registers being mapped to one of the banks in the data memory, wherein one of the special function registers is a working register being coupled with the arithmetic logic unit;

a program counter register within the central processing unit, the program counter mapped in the data memory; and

a working register within the central processing unit being coupled with the arithmetic logic unit, the working register mapped in the data memory;

wherein the microcontroller having an instruction set for controlling the arithmetic logic unit;

wherein at least one instruction comprises a bit indicating whether the bank select unit accesses one of the banks or the virtual bank; and

wherein the instruction set includes an instruction with an encoding of 0000 0000 0001 0100, wherein upon invocation of the instruction, the values from a first register are copied into an upper 16 bits of a program counter and a value in a second register are copied into a lower 8 bits of the program register.

11. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

12. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1010 kkkk kkkk, wherein upon invocation of the instruction, an 8 bit literal is copied to the location pointed to by a file select register, and the file select register is then decremented, the literal 'k' is designated in the kkkk kkkk portion of the instruction.

13. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1001 ffkk kkkk, wherein upon invocation of the instruction, a 6 bit unsigned literal is subtracted from a file select register to form a result, the result being stored into the file select register, the literal being designated in the kk kkkk portion of the instruction, the file select register begin designated in the ff portion of the instruction.

14. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1001 11kk kkkk, wherein upon invocation of the instruction, an unsigned 6 **[[big]]** **bit** literal is subtracted from a file select register to form a result, the result being stored back into the file select register and returned, the literal being designated in the kk kkkk portion of the instruction.

15. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1000 ffkk kkkk, wherein upon invocation of the instruction, an unsigned 6 bit literal is added to a file select registered, the result being stored into the file select register, the literal being designated in the kk kkkk portion of the instruction, the file select register being designated in the ff portion of the instruction.

16. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1000 11kk kkkk, wherein upon invocation of the instruction, a 6 bit literal designated by the kk kkkk portion of the instruction is added to a file select register and the result is stored back into the file select register.

17. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1011 0sss ssss 1111 dddd dddd dddd, wherein upon invocation of the instruction, an 8 bit value is copied to a destination designated by the 12 bit value dddd dddd dddd, the location of the 8 bit value that is copied to the destination is designated by adding the 7 bit literal value sss ssss to the value in a file select register.

18. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 1110 1011 1sss ssss 1111 xxxx xddd dddd, wherein upon invocation of the instruction, an 8 bit value is copied to a location designated by ddd dddd portion of the instruction, the location of the 8 bit value is determined by adding the 7 bit literal value sss ssss to the value in a file select register.

19. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 0000 0000 0001 0100, wherein upon invocation of the instruction, an address of a next instruction is pushed onto a hardware stack.

20. **(currently amended):** A microcontroller ~~**as in claim 11**~~ **comprising:**

a central processing unit;

a data memory coupled with the central processing unit being divided into n banks;

the central processing unit comprising:

a bank select unit for selecting one of the banks in the data memory, wherein the selected bank forms a register file;

an arithmetic logic unit coupled with the register file; and

a plurality of special function registers being mapped to one of the banks in the data memory;

wherein one of the special function registers is a working register being coupled with the arithmetic logic unit; and

wherein the instruction set includes an instruction with an encoding of 0000 0000 0001 0100, wherein upon invocation of the instruction, the values from a first register are copied into an upper 16 bits of a program counter and a value in a second register are copied into a lower 8 bits of the program register.